IN THE SPECIFICATION

Please replace the paragraph beginning at page 1, line 30, with the following:

In U.S. Patent No. 5,535,357, issued to Moran et al., entitled "Flash memory system providing both BIOS and user storage capability", an example of a flash memory used as a booting memory is disclosed. Referring to FIG. 1, in order to use a NAND flash memory as the booting memory, a flash controller 8 performs an interfacing between a NAND flash memory 4 and a system bus 2. Here, the NAND ~~flash memory 9~~ flash memory 4 has to store a separate emulation means. The emulation means is indicative of means for using a region of the NAND flash memory as the hard disk. The flash controller 8 intercepts the BIOS booting process and installs the emulation means in a system memory 3. In the construction of FIG. 1, the system booting is performed as follows.

Please replace the paragraph beginning at page 10, line 22, with the following:

First, if the system controller 11 provides the interface unit 20 with information on address of the NAND flash memory 10 and information on the page number to be programmed, and also commands the interface unit 20 to program the NAND flash memory 10 (S41), the data corresponding to the to-be-programmed pages are loaded into the buffer unit 23. In other words, the program configuration information is provided to the register unit 22 of the interface unit 20 (PCS), and the data of the to-be-programmed pages are sequentially loaded into the buffer unit 23 (LPn, LPn+1, and LPn+2). Then, according to the order loaded into the buffer unit 23, program command and address with respect to a first page is provided (PCAn), corresponding data are loaded from the buffer unit 23 (Ln), and a program operation to the assigned page is executed (Pn) (S42). Here, as can be seen from the timing state ~~of FIG. 9,~~ of FIG. 11, it should be noted that data of the next page (e.g., N+1) is loaded into the buffer unit 23 while the program operation is executed to a current page (e.g., N). If the program operation to the current page is completed (S43), the interface unit 20 performs the program operation to the next page (N+1), which is stored in the buffer unit 23, just like the program operation to the first page ~~(PCAn+1 à Ln+1 à Pn+1)~~ (PCAn+1, Ln+1, Pn+1) (S45). If the program operation to the next page (i.e., the second page) is completed (S46), the system controller 11 checks whether or not the program operations are performed as many as the page number (e.g., three pages N to N+2) which is set to the interface unit 20 (S48). If not, the process proceeds to the step S45 so that the program operations to next pages are repeated.